Phase Locked Loop

RIBPL01

Key Features

- **Low Phase Noise, phase Locked Loop**
- **On-Chip VCO tunes from 2000 MHz to 2800 MHz**
- **Prescaler 4/5**
- **Programmable Divider (16-127 division)**
- **Low dynamic power consumption in locked state**
- **Duty cycle (45% to 55%).**
- **Temperature stability (-40 to +125 ^{0}C)**

Applications

- **ASIC clock generator**
- **Clocking of A/D and D/A converters**
- **Cellular Systems**
- **WLAN Systems**

General Description

The **RIBPL01** is a low power and fast locking phase lock loop utilizing 0.18um CMOS process technology to obtain high frequency operation both in the phase comparator and VCO sections. The device can be used as clock generator to provide the high speed clock signals in ASIC and various systems like WLAN, cellular.

The PLL provides a multi-output clock distribution function with subpicosecond jitter performance, along with an on-chip VCO. The on-chip VCO tunes from 2000 MHz to 2800 MHz.

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The Block Diagram shows the scheme that generates VCO clock frequency from 2000M to 2.8 GHz. In this PLL we have used Phase Frequency Detector, Charge Pump, Low Pass Filter, Ring Oscillator as a VCO, programmable divider gives division ratio of 16 to 127.

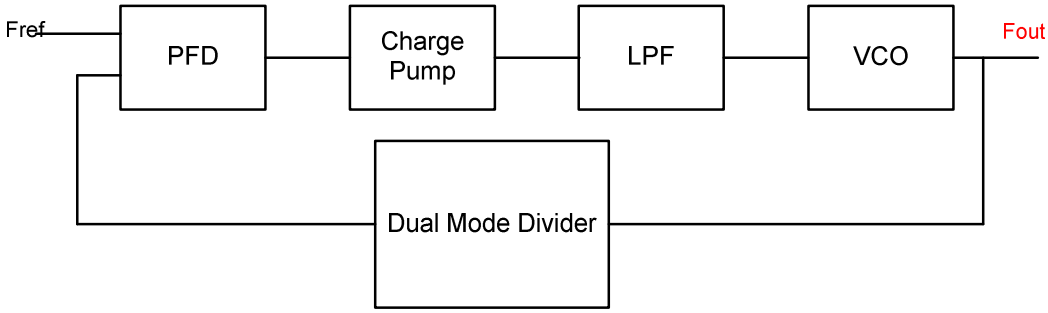


FIGURE 1: Functional Block Diagram

AC Electrical Characteristics

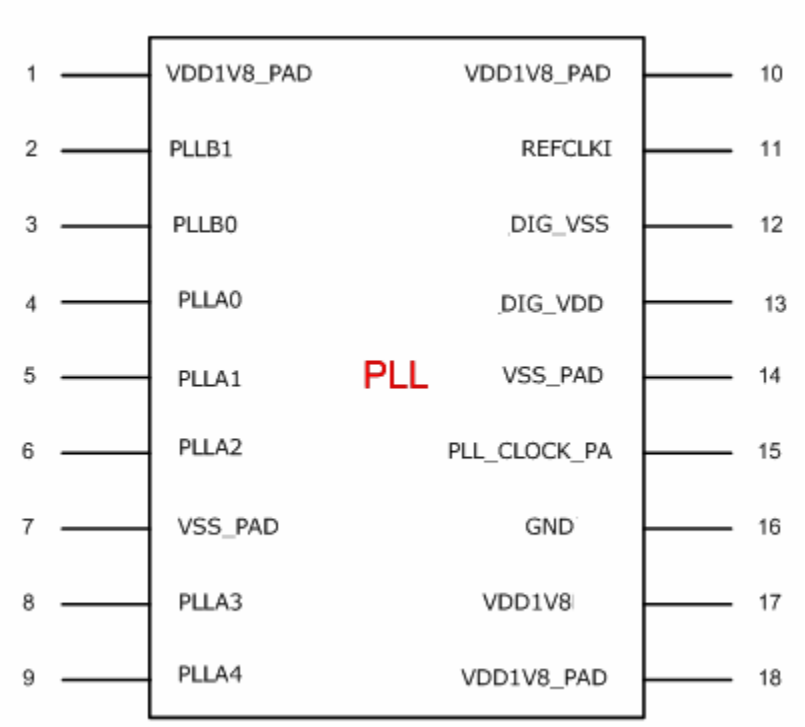
Typical (typ) is given for Vcc = 1.8 V ± 5%; TA = 25°C. Minimum (min) and Maximum (max) values are given over full Vcc and TA (−40°C to +125°C) variation.

	Descriptions	**Min.**	**Typ.**	**Max.**	**Units**
VCO	Frequency Range	2000		2800	MHz
	VCO Gain (Kvco)		667		MHz/V
	Tuning Voltage	0.6		1.8	V
Phase Frequency Detector (PFD)	PFD frequency	40			MHz
Charge Pump	Icp Source/sink	50		200	uA
Dual Mode Divider	Division Range	16		127	

TIMING CHARACTERISTICS

Descriptions	Min.	Typ	Max.	Units
Output Rise Time (Tr)		150	300	ps
Output Fall Time (Tf)		150	300	ps

PLL IC Pin Diagram & Description



Pin No	Pin Name	Description	Status	Min.	Max.	Signal behavior
1	VDD1V8_PAD	External Supply input Pin for 1.8V	Input	1.7 V	1.9 V	DC
2	PLLB1	Control Pin2 for dual mode divider for frequency division	Input	0	1.98 V	DC
3	PLLB0	Control Pin1 for dual mode divider for frequency division	Input	0	1.98 V	DC
4	PLLA0	Control Pin0 for dual mode divider for frequency division	Input	0	1.98 V	DC
5	PLLA1	Control Pin1 for dual mode divider for frequency division	Input	0	1.98 V	DC
6	PLLA2	Control Pin2 for dual mode divider for frequency division	Input	0	1.98 V	DC
7	VSS_PAD	External Ground input Pin	Input	0 V	50 mV	DC
8	PLLA3	Control Pin3 for dual mode divider for frequency division	Input	0	1.98	DC
9	PLLA4	Control Pin4 for dual mode divider for frequency division	Input	0	1.98	DC
10	VDD1V8_PAD	External Supply input Pin for 1.8V	Input	1.7 V	1.9 V	DC
11	REFCLKI	Reference Crystal Clock Input at 20MHz for PLL	Input	0	1.98 V	20 MHz
12	DIG_VSS	Dedicated Digital Ground Pin for PLL	Input	0	50 mV	DC
13	VDD	Dedicated Digital Voltage supply of 1.8V for PLL	Input	1.7	1.98 V	DC
14	VSS_PAD	External Ground input Pin	Input	0 V	50 mV	DC
15	PLL_CLOCK_ PA	PLL -CLOCK	output			2.4 GHz
16	GNDPLL	Dedicated Analog Ground Pin for PLL	Input	0 V	50 mV	DC
17	VDD1V8	Dedicated Analog Voltage supply of 1.8V for PLL	Input	1.7 V	1.9 V	DC

18	VDD1V8_PAD	External Supply input Pin for 1.8V	Input	1.7 V	1.9 V	DC

PLL Simulation Results

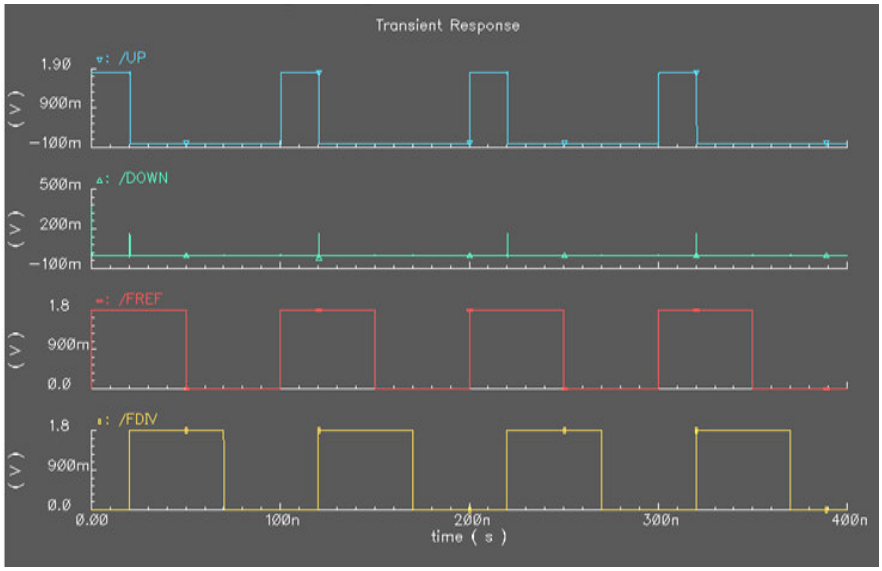


FIGURE 2 : PFD Result (Reference Frequency > Feedback Frequency)

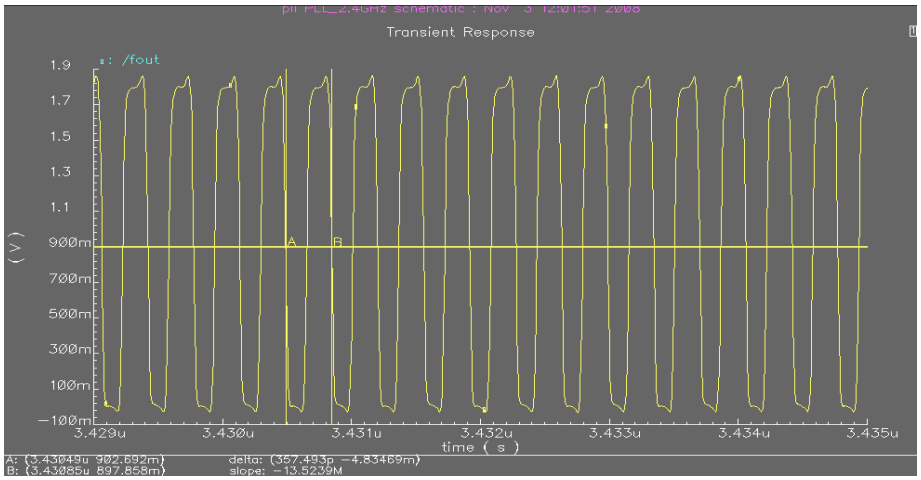


FIGURE 3: VCO Simulations Result at 2.8 GHz

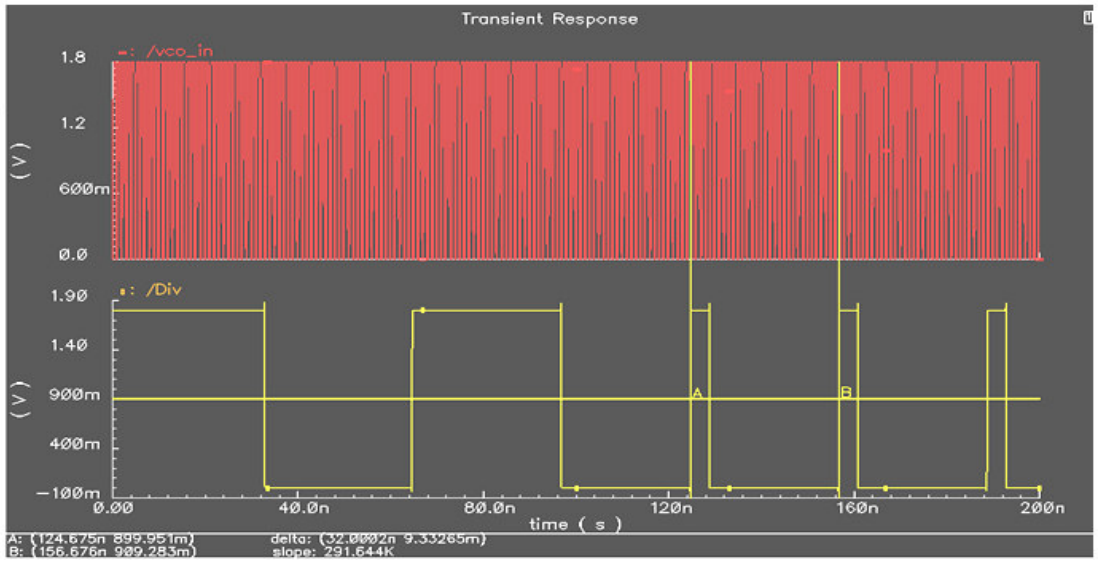


FIGURE 4: Dual Modulus Divider Result

(Divide by 32)

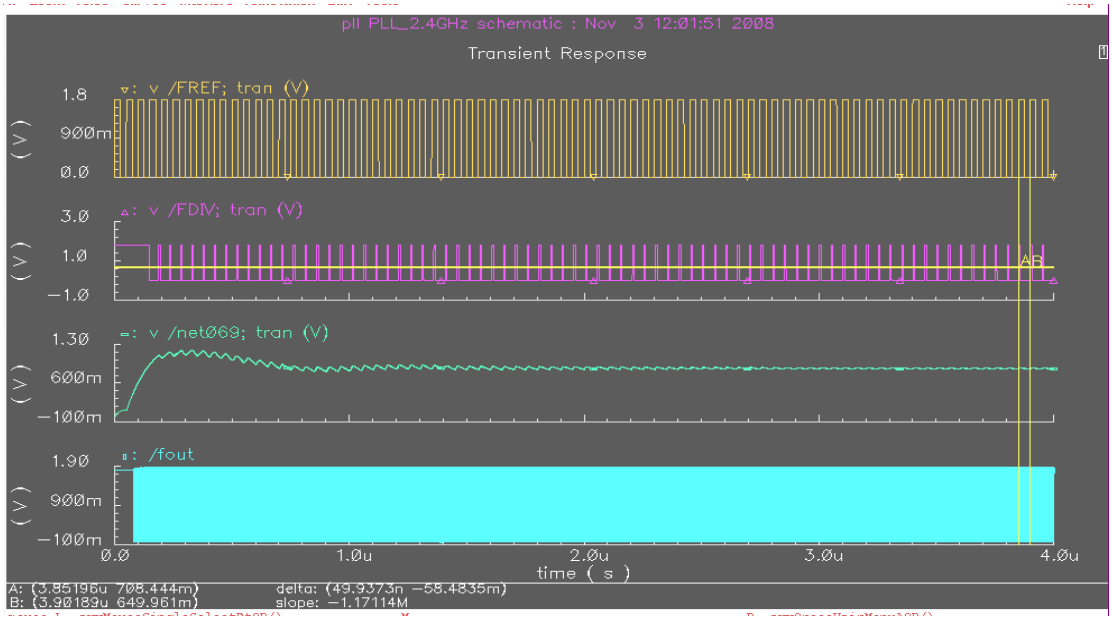


FIGURE 5: PLL results in locked condition for division ratio of 70

Phase Locked Loop

Configuration of PLL

The Design allows flexible configuration of the PLL, accommodating various reference frequencies, PFD comparison frequencies, VCO frequencies, internal VCO. This is accomplished by the various settings that include the 5 bit divider, the 2 bit divider, the PFD polarity, the charge pump current and the loop bandwidth. These are managed through programmable Divider settings. Successful PLL operation and satisfactory PLL loop performance are highly dependant upon proper configuration of the PLL settings. The design of the loop filter is crucial to the proper operation of the PLL. A thorough knowledge of PLL theory and design is helpful.

Phase Frequency Detector (PFD)

The PFD takes inputs from the Dual Mode counter and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer functions and minimizes phase noise and reference spurs. An important limit to keep in mind is the maximum frequency allowed into the PFD.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs, and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the internal VCO through the LF pin to move the VCO frequency up or down.

VCO

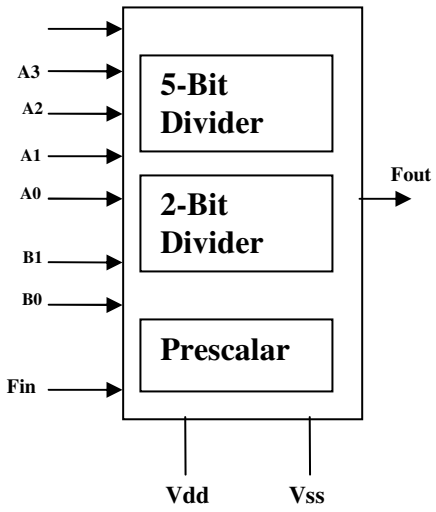
The PLL includes an on-chip VCO covering the frequency range (500 MHz to 1000 MHz). Achieving low VCO phase noise was a priority in the design of the VCO.

To tune over the wide range of frequencies covered by this VCO, ranges are used.

Reference Divider R

The reference inputs are routed to the reference divider, R. R (a 3-bit counter) can be set to any value from 0 to 8 The output of the R divider goes to one of the PFD inputs to be compared to the VCO frequency divided by the N divider. The frequency applied to the PFD must not exceed the maximum allowable frequency, which depends on the antibacklash pulse setting.

Feedback Divider N:



The N divider is a combination of a prescaler (P) and two counters, A and B. The total divider value is

$$N = (P \times A) + B$$

Where, the value of P can be 4 and 5 Prescaler

The prescaler of the PLL allows dual modulus (DM) mode operation where the prescaler divides by P and (P + 1) {4 and 5}.

When operating the PLL in dual modulus mode (P//P + 1), the equation used to relate input reference frequency to VCO output frequency is

$$fVCO = (fREF/R) \times (P \times A + B) = fREF \times N/R$$

A and B Counters

The 5-bit Divider:

A COUNTER is a 5-bit count down counter that can be programmed / loaded with a 5-bit programming word.

A0 and A4 are the 5 outputs of the TSPC- based D flip-flops (DFF), and these 5 outputs form the counter. A0 (LSB) always toggles at each positive clock edge, therefore, the counter counts down at every positive clock edge. 5 inputs to this circuit are the programmable inputs, and they go to the 5 MUXes that are controlled by the LOAD signals. When LOAD is high, the 5 inputs are programmed into the inputs of D flip flops. However, when LOAD is low, the MUXes transmit a feedback signal to the input of D flip flops. This feedback signal is generated by the XNOR gates and DFFs connected in series. XNOR gates are arranged such that when all the lower order flip flops are at logic low, the next higher flip flop toggles from its present state, otherwise the flip flop holds its present state. When the count signal is zero, the Zero- Detect Circuit generates a positive going edge that remains high until a programming word is loaded into the counter. LOAD signal controls the MUX operations and due to large fan-outs, the signal is buffered by a LOAD buffer circuit.

The 2-bit Divider:

The circuit operates the same way as the 5-bit programmable counter except the fact that it has a 2-bit counter and a 2- bit programming word only. The output of the Zero-Detect Circuit in the 2-bit programmable counter is the MODCONTROL signal used to control the divide modulus of the prescaler circuit.

The Programming Table for Dual Modulus Programmable Frequency Divider

Note:- A constraint in the two programmed input values is that A COUNTER (A4,A3,A2,A1,A0) value must always be greater than B COUNTER (B1,B2) value.

5 Bit Programming Word	Decimal (A)	2 Bit Programming Word	Decimal (B)	Prescaler P/P+1	Overall Division Ratio N=A.P +B

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A4	A3	A2	A1	A0		B1	B0		P = 4	
0	1	0	0	0	8	0	0	0	4	32
						0	1	1		33
						1	0	2		34
						1	1	3		35
0	1	0	0	1	9	0	0	0	4	36
						0	1	1		37
						1	0	2		38
						1	1	3		39
0	1	0	1	0	10	0	0	0	4	40
						0	1	1		41
						1	0	2		42
						1	1	3		43
0	1	0	1	1	11	0	0	0	4	44
						0	1	1		45
						1	0	2		46
						1	1	3		47
0	1	1	0	0	12	0	0	0	4	48
						0	1	1		49
						1	0	2		50
						1	1	3		51
0	1	1	0	1	13	0	0	0	4	52
						0	1	1		53
						1	0	2		54
						1	1	3		55
0	1	1	1	0	14	0	0	0	4	56
						0	1	1		57
						1	0	2		58
						1	1	3		59
0	1	1	1	1	15	0	0	0	4	60
						0	1	1		61
						1	0	2		62
						1	1	3		63
1	0	0	0	0	16	0	0	0	4	64
						0	1	1		65
						1	0	2		66
						1	1	3		67
1	0	0	0	1	17	0	0	0	4	68
						0	1	1		69
						1	0	2		70
						1	1	3		71
1	0	0	1	0	18	0	0	0	4	72
						0	1	1		73
						1	0	2		74
						1	1	3		75

1	0	0	1	1	19	0	0	0	4	76
						0	1	1		77
						1	0	2		78
						1	1	3		79
1	0	1	0	0	20	0	0	0	4	80
						0	1	1		81
						1	0	2		82
						1	1	3		83
1	0	1	0	1	21	0	0	0	4	84
						0	1	1		85
						1	0	2		86
						1	1	3		87
1	0	1	1	0	22	0	0	0	4	88
						0	1	1		89
						1	0	2		90
						1	1	3		91
1	0	1	1	1	23	0	0	0	4	92
						0	1	1		93
						1	0	2		94
						1	1	3		95
1	1	0	0	0	24	0	0	0	4	96
						0	1	1		97
						1	0	2		98
						1	1	3		99
1	1	0	0	1	25	0	0	0	4	100
						0	1	1		101
						1	0	2		102
						1	1	3		103
1	1	0	1	0	26	0	0	0	4	104
						0	1	1		105
						1	0	2		106
						1	1	3		107
1	1	0	1	1	27	0	0	0	4	108
						0	1	1		109
						1	0	2		110
						1	1	3		111
1	1	1	0	0	28	0	0	0	4	112
						0	1	1		113
						1	0	2		114
						1	1	3		115
1	1	1	0	1	29	0	0	0	4	116
						0	1	1		117
						1	0	2		118
						1	1	3		119
1	1	1	1	0	30	0	0	0	4	120
						0	1	1		120

						1	0	2		122
						1	1	3		123
1	1	1	1	1	31	0	0	0	4	124
						0	1	1		125
						1	0	2		126
						1	1	3		127

PLL Layout