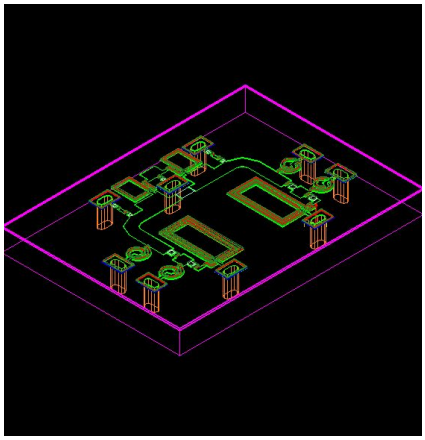
RFIC Solutions

Tech Brief

MMIC LAYOUT

What is the MMIC layout?

MMIC layout is the representation of an integrated circuit in terms of planar geometric shapes, which correspond to the patterns of metal, oxide or semiconductor layers that make up from components of the integrated circuit.



When using a standard layout process, where the interaction of the many thermal and photographic basic electronic components (active and passive) is known and carefully controlled the behavior of the final integrated circuit depends largely on the positions and interconnections of these basic electronic components.

In the earlier, simpler, days of IC design, layout was done by hand using opaque tapes and films, much like the early days of printed circuit board (PCB) design. Modern IC layout is done with the aid of IC layout editor software, mostly automatically using EDA, ADS, cadence tools, including place and route tools or schematic-driven layout tools. The manual operation of choosing and positioning the geometric shapes is informally known as "polygon pushing".

Using a computer-aided layout tool, the layout engineer or layout technician places and connects all of the components that make up the chip such that they meet certain criteria typically, which includes performance, size, density, and manufacturability shown in figure.

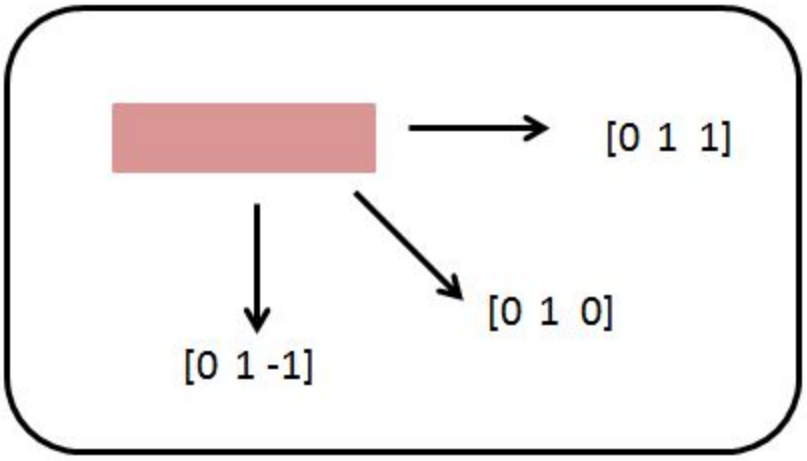
The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are given as:-

- design rule checking (DRC),
- layout versus schematic (LVS),
- parasitic extraction,

When all verification is complete, then layout is transferred into semiconductor foundry for processing the IC. Typically layout is sent GDSII format to a semiconductor foundry. The process of sending layout to the foundry is called tapeout because the data used to be shipped out on a magnetic tape. The foundry converts the data into another format and uses it to generate the photomasks used in a photolithographic process of semiconductor device fabrication.

What are the general layout design rules?

- Set snap and grid spacing 0.1um. By making the grid visible, you can draw shapes with exact size and spacing.
- Set up your layer definitions. Specify the drawing layer. All shapes are entered on layers. The color and visibility of any shape is controlled by the layer on which it is drawn. Before you begin drawing.
- When you create a layout directly, you place components or shapes in the Layout window. You can select components from either the palette or the library list and place it at designating coordinates.
- Gates must be oriented along the [0 1 1] reciprocal lattice as shown in the figure below.
- Geometries must be designed on 0.1 um grid except gate on 0.05 um grid.
- Device gate width is defined by ohmic contact width for transistors with gate width larger than 10 um but for very small devices (gate width < 10 um).
- The minimum die size considered according to standard package of selected foundry.
- The aspect ratio of chip dimension should be equal or less than 3:1.
- The design only use base layer for labeling, other layers is not used.



- The overall layer to layer minimum spacing is 2.0um
- Transistors source & drain and layer spacing length is 2.0um fixed.

- Between Two Layer minimum spacing length is 5um.
- Minimum layer length is 5um.
- Airbridge consider 2different layer. In airbridge one layer1 consider maximum width is 20um and layer2 consider maximum width 10um respectively.
- Between two grounds 50um distance is needed by keeping fixed Ground size.
- Placing of Diode and Transistor is always horizontal, not allowed to do vertical.
- Consider all interconnection between two components in schematic.
- Interconnect two components by transmission line not by metal.
- For junction connection use Tee, Cross, Bend, smooth curve
- For two cross-connection use airbridge
- If 50ohm width is greater than minimum airbridge width then use tapper after airbridge. It provides
- When a component is placed in the Layout window, note that each pin of component is outlined and glow in layout. When two pins of 2 different component are connected, the outline disappears. As described in following figure 2, review the highlight color of pins as well as the color of connections.

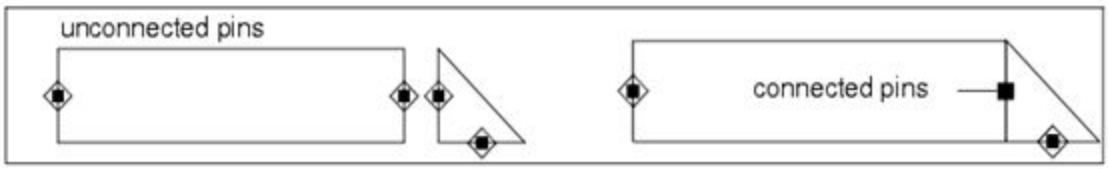


Figure 2:-how to connect to two components

- For symmetry blocks, layout symmetry is important.
- When transmission lines are required to bend (change direction) due to routing constraints, use a bend radius that is at least 3 times the center conductor width. In other words: - Bend Radius ≥ 3 × (Line Width). It provides minimum any characteristic impedance by changes moving through the bend.

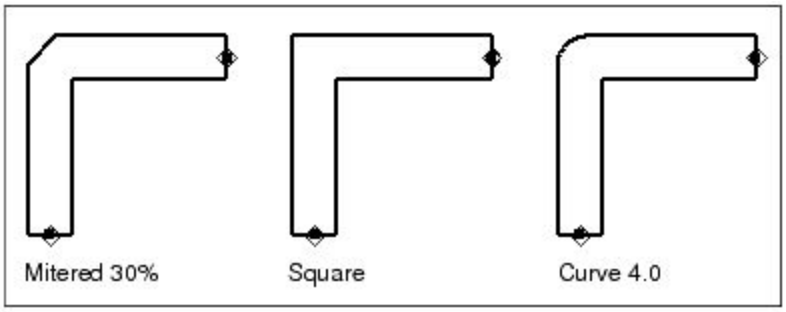


Figure 3:- Different bend types

➢ Where a gradually curved bend is not possible, the transmission line can undergo a right-angle bend, see figure 1. However, this must be compensated to reduce the impedance discontinuity caused by the local increase in effective line width going through the bend. A standard compensation method is the angled miter, as shown below. The optimum microstrip right-angle miter is given by the formula:-

$$M = 100\frac{x}{d}\% = (52 + 65e^{-\frac{27w}{20h}})\%$$

Where M = fraction (%) of the miter compared to the non mitered bend. Above formula will be employed for other transmission lines. If there is any uncertainty as to the correct compensation, then bend should be modeled using an electromagnetic simulator if the design requires high performance transmission lines.

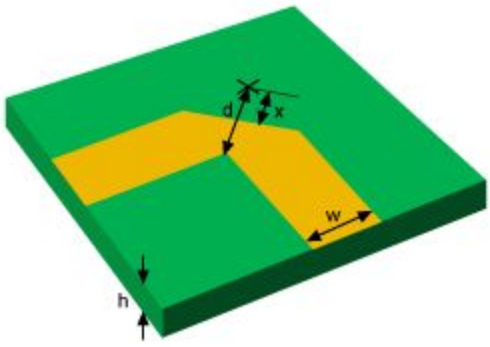
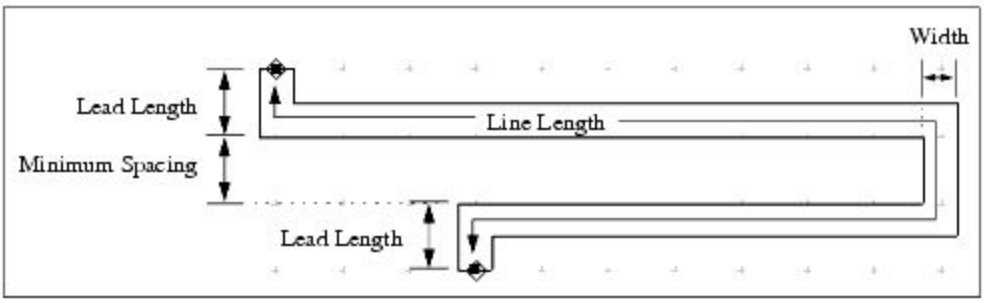


Figure 4:- The transmission line can undergo a right-angle bend.

- Traces are wires with width and a bend type. Which are used to represent physical transmission lines. Like wires, they can be used to connect components. For simulation purposes, there is no difference between a trace connection and a wire connection. Traces are normally simulated as simple connections (shorts). However they can be converted to or simulated as transmission lines, to allow for more accurate simulation.
- Explicitly convert them to transmission lines (Edit > Path/Trace>Convert Traces). In this case, the selected traces are actually removed and replaced by an equivalent transmission line component in the layout itself.

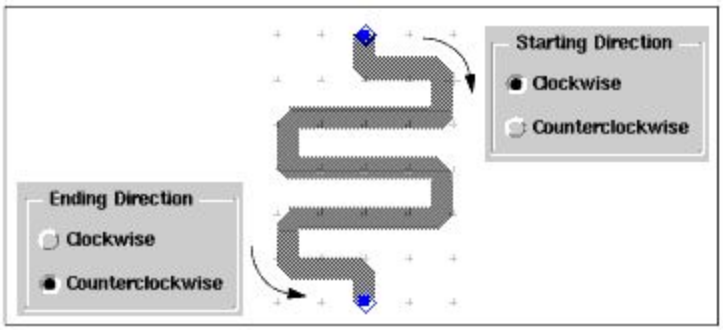
Figure 5:-How traces shows connection in schematic after converting all traces by transmission line

- Simulate them as transmission lines without actually converting them. In this case, the traces are not replaced, but an underlying subnetwork is created for each one, and that subnetwork contains the equivalent transmission line. The subnetwork creation occurs during the Design Synchronization process (Generate/Update). For details, refer to Simulating Traces as Transmission Lines.
- Meander traces enable you to quickly insert traces with specific characteristics including length, spacing, and orientation.



- Corner Type - Select from Mitered, Square, Curve
- Starting Direction - The direction (clockwise or counterclockwise) in which the first two segments connected to the starting lead are drawn.

- Ending Direction - The direction (clockwise or counterclockwise) in which the last two segments connected to the ending lead are drawn.



- Width - The desired width for the trace.
- Minimum Spacing - The minimum spacing between the parallel trace segments.
- Line Length - The total length of the trace, including the lead length segments.
- Mitered Corner Cutoff Ratio (%) - The desired cutoff ratio for the corner type Mitered.
- Curve Radius - The desired curve radius for the corner type Curve.
- Lead Length - The length of the starting and ending segments.
- Meanders Line Orientation - Select vertical if you want the trace to meander vertically between the specified starting and ending leads; select horizontal if you want the trace to meander horizontally between the specified starting and ending leads.

Layout versus Schematic (LVS),

` Design Verification After layout is completed, it is often necessary to have an independent check, i.e. reverse engineering. This will minimize human error of circuit layout. In low frequency analogue design, software tools are now available commercially to implement automatic layout. This significantly reduces design time. However, for RF and Microwave design such tools are only available for a limited range of foundries, which is developed internally by foundry. One way to verify the design is to have an independent person who takes the layout and translates the content into a schematic, which is turn in simulated circuit. Then compare result with the designed one and modified both schematic as well as layout. This process is done for to cut down the un-avoidable human error. Design rules are also checked at this point to ensure all foundry layout rules have been followed. This reverse engineering process can now be carried out automatically using a software tool, e.g. Cadence, ADS. This process is called layout verses schematic (LVS). During LVS process the software recognizes the layout patterns and translates them into schematics for circuit simulations. The schematics and simulations can then be compared manually. This Process Verify that schematic and layout have equal component, see in fig 6.

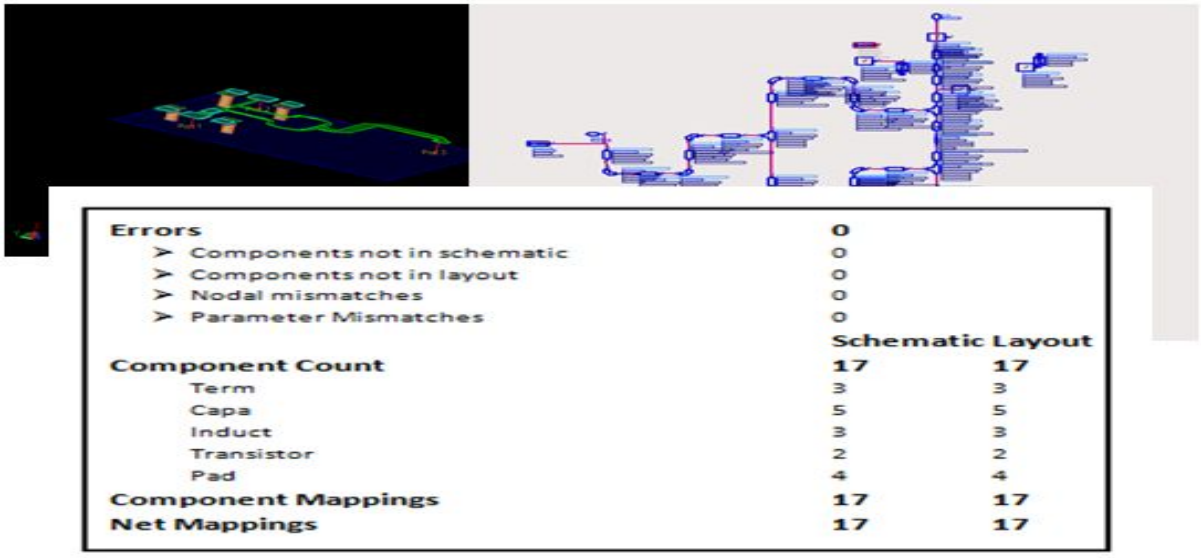


Figure 6:- Layout Vs Schematic(LVS)

Parasitic Extraction

In electronic design automation, parasitic extraction is calculation of the parasitic effects in the designed devices when they are interconnects in layout shows : parasitic capacitances, parasitic resistances and parasitic inductances, commonly called parasitic components or simply parasitic.

The major purpose of parasitic extraction is to create an accurate analog model of the circuit by using layout vs schematic method. Actual simulations can emulate RF analog circuit responses with consideration of all parasitic.

In early integrated circuits the impact of the interconnection was negligible because layout considers lots of space it is not compact version. Between two components considers lots of space according to parasitic effect. There is no coupling effect occurred. So chips are in larger in size.

Interconnection of node resistance and capacitance in the 0.5-micrometre technology node shows a significant impact on circuit performance. With shrinking of chip size effects of interconnects became important as well. There are some effects of interconnect parasitic include: signal delay, signal noise etc.